APPENDIX A

DEVICE FOR CONTROLLING A SETUP/HOLD TIME OF AN INPUT SIGNAL

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] The present invention generally relates to a device for controlling a setup/hold time of an input signal, and more specifically, to a technique to control the setup/hold time of various control signals applied from an input buffer without physically changing the control device.

2. Description of the Prior Art

[0002] Fig. 1 is a circuit diagram illustrating a conventional device for controlling setup/hold time of input signal.

[0003] The conventional device for controlling a setup/hold time of an input signal comprises inverters IV1~IV4 for performing a driver function, MOS capacitors C1~C4 for performing a signal delay function, metal option unit 2 and 3, and a latch 4.

[0004] Here, the inverters IV1 and IV2 output signals by driving an address, a command signal or input data applied from an input buffer 1. The inverter IV3 outputs a signal by driving an output signal of the metal option unit 2.

The inverter IV4 drives an output signal of the metal option unit 3 to provide a global bus line control signal GB_BL to the latch 4.

[0005] The metal option units 2 and 3 comprising metal option switches MO1~MO4 selectively control the MOS capacitors C1~C4 to control setup/hold time of the global bus line control signal GB_BL.

[0006] The MOS capacitors C1 and C2 are selectively connected to an output terminal of the inverter IV2 by the metal option switches MO1 and MO2. The MOS capacitors C3 and C4 are selectively connected to an output terminal of the inverter IV3 by the metal option switches MO3 and MO4.

[0007] The latch 4 latches the global bus line control signal GB_BL in synchronous to a clock signal CLK to output the latched signal into a global bus line (not shown). Here, in order that the global bus line control signal GB_BL inputted into the latch 4 may be valid, the global bus line control signal GB_BL should be transmitted into the latch earlier than the clock signal CLK by a predetermined time (setup time). When the latch 4 performs a latch operation in synchronous to the clock signal, a state of the global bus line control signal GB_BL should be maintained for a predetermined time (hold time).

[0008] Here, the ideal condition is that the clock signal

CLK is enabled after the setup time of the global bus line control signal GB_BL has passed, and the state of the global bus line control signal GB_BL for the hold time has been maintained.

[0009] However, it is difficult to satisfy the above ideal condition because signals inputted from outside of an actual chip through the input buffer 1 are influenced by length of an internal transmission line, various noises, capacitance or resistance, and so forth.

[0010] Accordingly, the device for controlling a setup/hold time of an input signal is designed to control the setup/hold time of the global bus line control signal GB_BL by selectively connecting signal delay devices such as the MOS capacitors C1~C4.

[0011] In other words, the metal option switches MO1~MO4 requiring physical apparatus are used to regulate the setup/hold time of the global bus line control signal GB_BL. As a result, since circuits of metal layers need to be physically changed to regulate the setup/hold time, the conventional device has a problem consuming a long time and a high cost .

SUMMARY OF THE INVENTION

[0012] The present invention is directed to a device for

controlling a setup/hold time of an input signal that controls a setup/hold time of various control signals applied to a global bus line according to a decoded test mode control signal.

[0013] There is provided a device for controlling a setup/hold time of an input signal, comprising: a driver for outputting a global bus line control signal by amplifying an output signal from an input buffer, a signal delay unit for delaying the global bus line control signalselectively connected to the driver, a decoding unit for outputting a test mode delay signal by decoding a test control signal for determining to control setup/hold time corresponding to the global bus line control signal, a test mode entry signal, and a test mode exit signal, and a delay control unit for controlling the setup/hold time of the global bus line control signal by selectively connecting the signal delay unit to the driver according to a state of the test mode delay signal.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] Fig. 1 is a circuit diagram illustrating a conventional device for controlling a setup/hold time of an input signal .

[0015] Fig. 2 is a circuit diagram illustrating a device for

controlling a setup/hold time of an input signal according to an embodiment of the present invention.

[0016] Fig. 3 is a circuit diagram illustrating a decoding unit according to an embodiment of the present invention.

[0017] Fig. 4 is a timing diagram illustrating operation of a device for controlling a setup/hold time of an input signal according to an embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0018] The present invention will be described in detail referring to the accompanying drawings.

[0019] Fig. 2 is a circuit diagram illustrating a device for controlling a setup/hold time of an input signal according to an embodiment of the present invention.

[0020] Referring to Fig. 2, the device for controlling a setup/hold time of an input signal of the present invention comprises a driver 20, signal delay units 30 and 40, delay control units 50 and 60, and a latch 70.

[0021] The driver 20 comprises inverters IV5~IV8 for outputting a global bus line control signal GB_BL into a latch 70 by driving an address, a command signal or input data applied from an input buffer 10. Here, the inverters IV5 and IV6 output signals by driving an output signal of the input buffer 10. The inverter IV7 outputs a signal by

driving an output signal of the delay control unit 50. The inverter IV8 drives an output signal of the delay control unit 60 to provide the global bus line control signal GB_BL to the latch 70.

[0022] The signal delay unit 30 comprises MOS capacitors C5 and C6 selectively connected to an output terminal of the inverter IV6 controlled by the delay control unit 50. The signal delay unit 40 comprises MOS capacitors C7 and C8 selectively connected to an output terminal of the inverter IV7 controlled by the delay control unit 60.

[0023] The delay control unit 50 comprising an inverter IV9 and transmission gates T1 and T2 selectively connects MOS capacitors C5 and C6 to control the setup/hold time of the global bus line control signal GB_BL provided to the latch 70. The inverter IV9 inverts a test mode delay signal TM_DLY<0>. The transmission gates T1 and T2 selectively connects the MOS capacitors C5 and C6 to the output terminal of the inverter IV6 according to a state of the test mode delay signal TM_DLY<0>.

[0024] Here, the transmission gates T1 and T2 receive the test mode delay signal TM_DLY<0> through a NMOS gate, and the inversion of the test mode delay signal TM_DLY<0> by the inverter IV9 through a PMOS gate.

[0025] The delay control unit 60 comprising an inverter IV10

and transmission gates T3 and T4 selectively connects MOS capacitors C7 and C8 to control the setup/hold time of the global bus line control signal GB_BL provided to the latch 70. The inverter IV10 inverts a test mode delay signal TM_DLY<1>. The transmission gates T3 and T4 selectively connects the MOS capacitors C7 and C8 to the output terminal of the inverter IV7 according to a state of the test mode delay signal TM_DLY<1>.

[0026] Here, the transmission gates T3 and T4 receive the test mode delay signal TM_DLY<1> through a PMOS gate, and the inversion of the test mode delay signal TM_DLY<1> by the inverter IV10 through a NMOS gate.

[0027] The latch 70 latches the global bus line control signal GB_BL in synchronous to a clock signal CLK to output the latched signal into a global bus line (not shown).

[0028] Fig. 3 is a circuit diagram illustrating a decoding unit for generating the test mode delay signal TM_DLY<0> of Fig. 2.

[0029] The decoding unit comprises a logic unit 80 and latches 90 and 100. The logic unit 80 logically operates a test control signal TCS and a test mode entry signal TM_EP. The latches 90 and 100 latches output signals of the logic unit 80 and an test mode exit signal TM_EXP to output a test mode delay signals TM_DLY<1:0>.

[0030] Here, the logic unit 80 comprises an inverter IV11 and NAND gates ND1 and ND2. The inverter IV11 inverts a test control signal TCS. The NAND gate ND1 NANDs the test control signal TCS and the test mode entry signal TM_EP. The NAND gate ND2 NANDs the test mode entry signal TM_EP and an output signal of the inverter IV11.

[0031] The latch 90 comprises two cross-coupled NAND gates ND3 and ND4 with an output of a NAND gate fed back to an input of the other NAND gate. A NAND gate ND3 NANDs an output signal of the NAND gate ND1 and an output signal of the NAND gate ND4 to output the test mode delay signal TM_DLY<0>. The NAND gate ND4 NANDs the test mode exit signal TM_EXP and an output signal of the NAND gate ND3.

[0032] The latch 100 comprises two cross-coupled NAND gates ND5 and ND6 with an output of a NAND gate fed back to an input of the other NAND gate. The NAND gate ND5 NANDs an output signal of the NAND gate ND2 and an output signal of the NAND gate ND6 to output the test mode delay signal TM_DLY<1>. The NAND gate ND6 NANDs the test mode exit signal TM_EXP and an output signal of the NAND gate ND5.

[0033] The operation process of the device for controlling setup/hold time of input signal is described referring to Fig. 4.

[0034] In case of a normal operation mode, the test mode

delay signals TM_DLY<1:0> are maintained at a low state. When the test mode delay signal TM_DLY<0> is at a low state, the transmission gates T1 and T2 are all turned off, and outputs of the MOS capacitors C5 and C6 do not affect an output terminal of the inverter IV6. When the test mode delay signal TM_DLY<1> is at a low sate, the transmission gates T3 and T4 are turned on, and an output terminal of the inverter IV7 is connected to the MOS capacitors C7 and C8. AS a result, an output signal of the inverter IV7 is delayed by the MOS capacitors C7 and C8, and the global bus line control signal GB_BL is delayed.

[0035] In order to delay the setup/hold time of the global mode delay signal GB_BL in a test mode state, the decoding unit is controlled for the test mode delay signal TM_DLY<0> to be at a high level. On the other hand, in order to advance the setup/hold time of the global bus line control signal GB_BL, the delay unit is controlled for the test mode delay signal TM_DLY<1> to be at a high level.

[0036] When the test control signal TCS is at a high level, in order to delay the setup/hold time of the global bus line control signal GB_BL, the test mode entry signal TM_EP is enabled to a high level.

[0037] When the test mode entry signal TM_EP is enabled to the high level, the NAND gate ND1 of the logic unit 80

outputs a low signal, and the NAND gate ND2 outputs a high signal. Then, the latch 90 outputs the test mode delay signal TM_DLY<0> at the high level, and the latch 100 outputs the test mode delay signal TM_DLY<1> at the low level.

[0038] Thereafter, when the test mode delay signal TM_DLY<0> becomes high, the transmission gates T1 and T2 of the delay control unit 50 are all turned on, and an output signal of the inverter IV6 is delayed by the MOS capacitors C5 and C6. When the test mode delay signal TM_DLY<1> becomes low, the transmission gates T3 and T4 of the delay control unit 60 are all turned on, and an output signal of the inverter IV10 is delayed by the MOS capacitors C7 and C8.

[0039] Next, when a test mode exit signal /TM_EXP is generated, the test mode delay signal TM_DLY<0> is disabled to the low level, and maintained at a normal state.

[0040] As a result, when the test control signal TCS is at the high level, the test mode delay signal TM_DLY<0> becomes high to delay the setup/hold time of the global bus line control signal GB_BL.

[0041] On the other hand, when the test control signal TCS becomes low, the test mode entry signal TM_EP is enabled to the high level to advance the setup/hold time of the global bus line control signal GB_BL.

[0042] When the test mode entry signal TM_EP is enabled to the high level, the NAND gate ND1 of the logic unit 80 outputs a high signal, and the NAND gate ND2 outputs a low signal. Then, the latch 90 outputs the test mode delay signal TM_DLY<0> at the low level, and the latch 100 outputs the test mode delay signal TM_DLY<1> at the high level.

[0043] Next, when the test mode delay signal TM_DLY<0> becomes low, the transmission gates T1 and T2 of the delay control unit 50 are all turned off, and output signal of the inverter IV6 is not delayed. When the test mode delay signal TM_DLY<1> becomes high, the transmission gates T3 and T4 of the delay control unit 60 are all turned off, and an output signal of the inverter IV7 is not delayed.

[0044] Thereafter, when the test mode exit signal /TM_EXP is generated, the test mode delay signal TM_DLY<1> is disabled to the low level, and maintained at a normal state.

[0045] Accordingly, when the test control signal TCS is at the low level, the test mode delay signal TM_DLY<1> becomes high to advance the setup/hold time of the global bus line control signal GB_BL.

[0046] As discussed earlier, a setup/hold time control signal of the present invention can optimize the setup/hold time at a small cost by changing the setup/hold time of

control signals outputted from an input buffer without physically changing the control device.